REMARKS

This Amendment After Final Rejection is submitted in response to the outstanding final Office Action, dated July 30, 2004. Claims 1 through 36 are presently pending in the above-identified patent application. In this response, Applicants propose to amend claims 1, 13, 25, and 33. No additional fee is due.

This amendment is submitted pursuant to 37 CFR §1.116 and should be entered. The Amendment places all of the pending claims, i.e., claims 1 through 36, in a form that is believed allowable, and, in any event, in a better form for appeal. It is believed that examination of the pending claims as amended, which are consistent with the previous record herein, will not place any substantial burden on the Examiner.

In the Office Action, the Examiner rejected claims 1-9, 11-21, 23-30, and 32-34 under 35 U.S.C. §102(b) as being anticipated by Mittel et al. (United States Patent Number 5,610,558). The Examiner also indicated that claims 10, 22, 31, 35, and 36 would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

The present invention is directed to a gated clock recovery circuit that receives an input data stream and generates a frequency and phase aligned clock output. The gated clock recovery circuit substantially instantaneously adjusts the generated clock signal to phase changes in the incoming data stream. In addition, the gated clock recovery circuit generates the clock output signal using only transmitted non-predetermined data. The gated clock recovery circuit includes two PLL circuits. The first PLL (PLL1) adjusts to the frequency of the transmitter, and provides a bias voltage, CAP1, to the second PLL (PLL2) to indirectly initially tune the second PLL. The bias voltage, CAP1, is applied to the second PLL through a transmission gate (or switch) that is initially in a closed (short) position. Thus, the first PLL drives the bias voltage, CAP2, of the second PLL, to align the frequency with the transmitter, until received data opens the transmission gate. Thereafter, the bias voltage, CAP2, is removed and the second PLL can operate without being controlled by PLL1 so that the second PLL oscillates in phase with the received data. Simultaneously, the received data starts the oscillator in the second PLL so that the second oscillator is in phase with the received data. The second PLL then maintains this phase relationship between the second oscillator and the received data.

Claims 1, 13, 15, and 33 have been amended to provide proper antecedent basis for the term "PLL."

Independent Claims 1, 13, 25, 26 and 33

Independent claims 1, 13, 25, 26 and 33 were rejected under 35 U.S.C. §102(b) as being anticipated by Mittel et al. Regarding claim 1, the Examiner asserts that Mittel discloses wherein said second PLL circuit has a second mode wherein said second PLL has an initial frequency determined by said bias signal and whereby said second PLL substantially instantaneously adjusts said clock output signal to phase changes of data in an input data stream (reference signal 147). The Examiner further asserts that the phrases "initial" and "substantially instantaneously" form a contradiction for the second mode signal operation, and that it is confusing and unclear as to how the second PLL instantaneously adjusts to an unbiased signal while having a bias signal at the same time.

Contrary to the Examiner's assertion, the phrases "initial" and "substantially instantaneously" do not form a contradiction for the second mode signal operation. For example, consider that the time interval of the second mode of operation is labeled t. Immediately after the bias signal is removed and the second PLL enters the second mode of operation, it has an initial frequency associated with the start of time interval t. This initial frequency was established by the bias signal that was utilized in the first mode. Thus, although the second PLL is in the second mode of operation and the bias signal has been removed, the frequency of the second PLL has been established by the bias signal. Following entry into this second mode of operation, the second PLL substantially instantaneously adjusts the clock output signal to phase changes of data in an input data stream without utilization of the bias signal, potentially changing the frequency from its initial value. Thus, the second PLL can have an initial frequency established by the bias signal and can substantially instantaneously adjust the clock output signal without utilizing the bias signal. Therefore, there is no contradiction between the phrases "initial" and "substantially instantaneously."

Applicants also note that Mittel teaches that

> the second filtered signal 321 is a current source signal that is combined with the tracking control signal 214. That is, the currents of these two signals are *added together* thereby creating a resultant current signal that coupled to the second oscillator 322.
> Col. 5, lines 22-26.

Tracking control signal 214 is generated by IDAC 330. IDAC 330 scales the oscillator control signal 212 generated by the master PLL 202 and *continuously* generates tracking control signal 214. Thus, the master PLL 202 continuously biases slave PLL 206. Mittel does not suggest or disclose that the master PLL 202 stops biasing the slave PLL 206. The independent claims, as amended, require that the bias signal generated by a first PLL is not used to bias a second PLL in a second mode.

Thus, Mittel et al. does not disclose or suggest that the bias signal generated by a first PLL is not used to bias a second PLL in a second mode, as required by independent claims 1, 13, 25, 26, and 33, as amended.

It is clear from the present specification that the bias signal is not operative to influence the second PLL in the second mode. The gated clock recovery circuit of the present invention includes two PLL circuits. The first PLL (PLL1) adjusts to the frequency of the transmitter, and provides a bias voltage, CAP1, to the second PLL (PLL2) to indirectly initially tune the second PLL. The bias voltage, CAP1, is applied to the second PLL through a transmission gate (or switch) that is initially in a closed (short) position. Thus, the first PLL drives the bias voltage, CAP2, of the second PLL, to align the frequency with the transmitter, until received data opens the transmission gate. Thereafter, the bias voltage, CAP2, is *removed* and the second PLL can operate without being controlled by PLL1 so that the second PLL oscillates in phase with the received data. Thus, the present amendment is supported by the original specification.

Dependent Claims 2-12, 14-24, 27-32 and 34-36

Dependent claims 2-9, 11-12, 14-21, 23-24, 27-30, 32, and 34 were rejected under 35 U.S.C. §102(b) as being anticipated by Mittel et al.

Claims 2-12, 14-24, 27-32 and 34-36 are dependent on claims 1, 13, 26, and 33, respectively, and are therefore patentably distinguished over Mittel et al. because of their dependency from amended independent claims 1, 13, 26, and 33 for the reasons set forth above, as well as other elements these claims add in combination to their base claim. The Examiner indicated that claims 10, 22, 31, 35, and 36 would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

All of the pending claims, i.e., claims 1-36, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully submitted,

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